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ABSTRACT OF THE INVENTION

Disclosed is a method for manufacturing an interconnect structure situated on a semiconductor wafer having a substrate assembly thereon. The interconnect structure is formed in a recess such as a trench, a hole, a via, or a combination of a trench and a hole or via within a dielectric material situated on the substrate assembly of the semiconductor wafer. At least one barrier layer is deposited within the recess. A seed layer helping to promote nucleation, deposition, and growth of a material that will be used to fill up the recess is then deposited on the barrier layer. An electrically conductive layer is then formed upon the seed layer. An energy absorbing layer will then be formed upon the conductor layer, where the energy absorbing layer has a greater thermal absorption capacity than that of the electrically conductive layer. The energy absorbing layer is heated, with or without an applied heightened pressure, to cause the conductor layer to flow so as to fill voids that have formed within the dielectric structure. Following the steps of heating or heating and pressurizing the energy absorbing layer, both the energy absorbing layer and a portion of the conductive layer situated above the dielectric structure are removed.

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